Please amend the claims as follows:

Amendments to the Claims

The following Listing of Claims will replace all prior versions and listings of Claims in the Application.

Listing of Claims

1. (Currently Amended) A memory system, comprising:

a cache system including a plurality of cache memories;

a requester input and a requester output, ~~each~~ responsive to selected ones of a plurality of requesters to request data from[[,]] the cache system and to store data to[[,]] the cache system, respectively;

a main memory to provide requested data that is not stored within the cache system;

cache tag logic;

a programmable storage device to store one or more indicators, different ones of the indicators selectively alterable for controlling different sequences of data transfers;

a control circuit coupled to the requester input and the requester output, the programmable storage device, the cache system, and to the cache tag logic, the control circuit

to receive data and to determine, based on the state of the one or more indicators, whether or not to update the cache tag logic to track the data, and

based on the state of the one or more indicators, to determine whether or not to store the data in the cache system, and if so, to replace the received data in the cache system.

2. (Cancelled)

3. (Previously Presented) The memory system of Claim 1, wherein one of the indicators indicates one of the cache memories is not available for use.

4. (Cancelled)

5. (Previously Presented) The memory system of Claim 1, wherein the main memory provides data to the cache system in response to a request that is any one of multiple request types, wherein at least one of the indicators identifies one or more of the request types, and wherein the control circuit prevents the replacement of the data in the cache if the data was provided in response to any of the identified request types.

6. (Currently Amended) The memory system of Claim 1, wherein the one or more request types includes a request type indicating the data will be modified by one of the plurality of requesters~~a requester~~.

7. (Currently Amended) The memory system of Claim 1, wherein at least one of the indicators identifies ~~one or more of the at least one~~ ones of the plurality of requesters, and wherein the control circuit replaces the data in the cache system if the data was returned from the main memory in response to a request issued by any of the identified ones of the plurality of requesters.

8. (Previously Presented) The memory system of Claim 1, wherein the main memory provides data to the cache system with a response that is any one of multiple response types, wherein at least one of the indicators identifies one or more of the response types, and wherein the control circuit replaces the data in the cache system if the data is returned from the main memory with any of the identified response types

9. (Previously Presented) A memory system, comprising:

a programmable storage device to store one or more indicators, different ones of the indicators adapted for controlling different sequences of data transfers;

a cache;

cache tag logic;

a control circuit coupled to the programmable storage device, the cache, and to the cache tag logic, the control circuit to receive data and to determine, based on the state of the

one or more indicators, whether or not to update the cache tag logic to track the data and whether to store the data to the cache; and

at least one requester coupled to the control circuit to return data to the cache tag logic, and wherein the control circuit determines whether or not to store the returned data to the cache based on the state of at least one of the indicators.

10. (Currently Amended) The memory system of Claim 9, wherein the at least one requester returns data to the cache tag logic during an operation that is any one of multiple operation types, wherein the indicators include an indicator to identify one or more of the operation types, and wherein the control circuit stores the returned data to the cache if the returned data is returned during any of the identified operation types.

11. (Original) The memory system of Claim 10, wherein the control circuit is further adapted to store the returned data to the cache based, at least in part, on whether a cache hit occurred.

12. (Original) The memory system of Claim 9, and further including a main memory coupled to the control circuit, and wherein the control circuit is adapted to forward the returned data to the main memory based, at least in part, on the state of at least one of the indicators.

13. (Original) The memory system of Claim 12, wherein memory coherency actions may be incomplete for the returned data or for associated data retained by the at least one requester or the cache, and further including a request tracking circuit coupled to the control circuit to prevent the returned data from being forwarded to the main memory until all of the memory coherency actions have been completed for the returned data or for the associated data.

14. (Previously Presented) The memory system of Claim 1, wherein the programmable storage device includes circuits to store microcode, and wherein the control circuit is controlled by the microcode.

15. (Previously Presented) The memory system of Claim 1, and further including mode switch logic coupled to the programmable storage device to automatically re-program at least one of the indicators in response to monitored conditions occurring within the memory system.

16. (Currently Amended) A method of controlling a memory system having cache tags to record which data is stored within one or more associated caches and a main memory coupled to the cache tags, and further having one or more programmable control indicators, comprising:

a.) obtaining data by providing a request for the data to, and receiving the data from, the main memory;

b.) determining whether or not to update the cache tags to record the data based on the state of one or more of the control indicators; and

c.) determining whether or not to store the data in a predetermined one of the associated caches based on the state of one or more of the control indicators;

wherein programmably altered control indicators affect ~~the either~~ at least one or both of the determinging steps; and

wherein the request is any one of multiple types, wherein one of the control indicators identifies one or more of the multiple request types, and wherein at least one of the determining steps is performed based, at least in part, upon whether the request is any of the identified response types.

17. (Cancelled)

18. (Cancelled)

19. (Cancelled)

20. (Previously Presented) The method of Claim 16, wherein the data is provided from the main memory with a response type that is any one of multiple response types, wherein one of the control indicators identifies one or more of the multiple response types, and wherein at least one of the determining steps is performed based, at least in part, upon whether the request is any of the identified response types.

21. (Previously Presented) The method of Claim 16, wherein the memory system is coupled to at least one requester, wherein one of the control indicators identifies one or more of the at least one requester, and wherein at least one of the determining steps is performed based, at least in part, upon whether the request was initiated by any of the identified requesters.

22. (Previously Presented) The method of Claim 16, wherein the memory system is coupled to at least one requester, and wherein step a.) includes obtaining the data from any one of the at least one requester.

23. (Original) The method of Claim 22, wherein the data is obtained during an operation that is any of multiple operation types, wherein one of the control indicators identifies one or more of the operation types, and wherein at least one of the determining steps is based, at least in part, on whether the data is obtained during any of the identified operation types.

24. (Original) The method of Claim 23, wherein at least one of the determining steps is based, at least in part, on whether a cache hit occurs.

25. (Previously Presented) The method of Claim 22, wherein the memory system includes a main memory, and further including providing the data to the main memory instead of storing the data into the predetermined one of the associated caches.

26. (Original) The method of Claim 25, wherein the data is associated with incomplete memory coherency actions, and further including preventing the data from being provided to the main memory until all incomplete memory coherency actions have been completed.

27. (Currently Amended) A method of controlling a memory system having cache tags to record which data is stored within one or more associated caches, and further having one or more programmable control indicators, comprising:

a.) obtaining data;

b.) determining whether to update the cache tags to record the data based on the state of one or more of the control indicators;

c.) monitoring conditions within the memory system; and

d.) automatically re-programming at least one of the one or more programmable control indicators based on one or more of the monitored conditions utilizing a selectively actuatable mode switch.

28. (Currently Amended) A memory system, comprising:

main memory means for storing data and for receiving requests to retrieve data;

cache means for storing a subset of the data;

programmable storage means for storing control indicators to determine how the subset of the data is to be selected, the programmable storage means further including means for selecting the subset of the data based, at least in part, on a type of request that was issued to retrieve the subset of the data from the main memory; and

one or more requester means for causing data to be retrieved from the main memory, and wherein the programmable storage means includes means for selecting the subset of the data based, at least in part, on the identity of one or more of the requester means that caused data to be retrieved from the main memory.

29. (Cancelled)

30. (Cancelled)

31. (Previously Presented) The memory system of Claim 28, wherein the main memory means for returning a response type to the cache means with data, and wherein the programmable storage means includes means for selecting the subset of the data based, at least in part, on the response type.

32. (Cancelled)

33. (Currently Amended) A memory system, comprising:

main memory means for storing data and for receiving requests to retrieve data;

cache means for storing a subset of the data;

programmable storage means for storing control indicators to determine how the subset of the data is to be selected, the programmable storage means further including means for selecting the subset of the data based, at least in part, on a type of request that was issued to retrieve the subset of the data from the main memory;

requester means for returning data to the cache means, and wherein the programmable storage means includes means for selecting whether data returned by the requester means will be stored to the cache means; and

wherein the requester means includes means for returning data during any of multiple types of operations, and wherein the programmable storage means includes means for selecting whether returned data will be stored to the cache means based, at least in part, on the type of operation that resulted in return of the data.

34. (Presently amended) The memory system of Claim [[32]]33, wherein the programmable storage means includes means for selecting whether data returned by the requester means will be stored to the cache means based, at least in part, on whether a cache miss occurred to the cache means.

35. (Original) The memory system of Claim 28, and further including mode switch means for modifying the state of one or more of the control indicators based on monitored conditions occurring within the memory system.

36. (Original) The memory system of Claim 28, and wherein the cache means includes cache tag means for tracking data that may be stored to the cache means, and wherein the programmable storage means includes means for determining whether to update the cache tag means to track data.

37. (Original) The memory system of Claim 36, wherein the programmable storage means includes means for enabling the tracking by the cache tag means of predetermined data that is not included in the subset of the data stored within the cache means.